ABSTRACT

A Packet Processor for a communication apparatus, for processing received and transmitted data streams made of packets, each packet mainly comprises a header and a payload section, comprising: **(A)** A receiving part comprising: A receiving PHY interface by which a flow of data stream is conveyed from a Modulator-Demodulator section of a modem to the Packet Processor; A receiving Tubular Bus receiving the said flow of data stream which is conveyed from the Modulator-Demodulator section of the modem to the Packet Processor, said receiving Tubular Bus conveying data, while processed, in the direction from the said receiving PHY interface to a host interface; At least one processing unit between sections of the said first Tubular Bus for sequentially receiving portions of a data stream from a section of the Tubular Bus, processing the same, and outputting the processed data to a next section of the said first Tubular Bus; One FIFO storage unit before and one FIFO storage unit after any of the said processing units on the receiving Tubular Bus, for providing a temporary storage for portions of the data stream; and A first host interface for receiving data from the receiving Tubular Bus and conveying it to a host. And **(B)** A transmitting part comprising: A second host interface for receiving data from the host and conveying it to a second Tubular Bus; A transmitting Tubular Bus for receiving the said flow of data stream which is conveyed from the host to the Packet Processor, said transmitting Tubular Bus conveying the data stream, while processed, in the direction from the said second host interface to a transmitting PHY interface; At least one processing unit between sections of the said transmitting Tubular Bus, for sequentially receiving portions of the data stream from a section of

the Tubular Bus, processing the same, and outputting the processed data to the next section of the said transmitting Tubular Bus; One FIFO storage unit before and one FIFO storage unit after any of the said processing units on the second Tubular Bus, for providing a temporary storage for portions of the data stream; and A transmitting PHY interface for receiving processed data from the transmitting Tubular Bus and conveying the same to a Modulator-Demodulator section. **(C)** A Backbone Bus for conveying management data, instructions, and addresses between various components of the Packet Processor; and **(D)** Timing and control means for administering the operation of the Packet Processor, and particularly the timing of using transmission slots for the transmit path.